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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,660	07/22/2003	Hisao Koyanagi	Q76637	4753

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,660	KOYANAGI, HISAO	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,8-12,15,19 and 20* is/are rejected.

7)☒ Claim(s) *3,5-7,13,14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

Status of Claims

Response to Amendment

Claims 1-18 were pending in this application. In response to the last Office Action, Claims 19-20 were added. Claims 1,4,11,15 32 were amended. As a result, claims 1-20 are remain pending in this application.

Claims 1-20 are in the application.

Claims 1-2,4,8-12,15,19-20 are rejected.

Claims 3,5-7,13-14,16-18 are objected.

Applicant's arguments filed 12/15/05 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the amendments

All rejections and objections not explicitly repeated below are withdrawn.

Specifications

The disclosure is objected to because of the following informalities:

Page 3, line 14 of specification, the recitation "..vector resistor.." should be "..vector register.."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2,8-12,19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al (US 6862676) in view of Suzuki (US 6240524).

As for claim 1, Knapp describes: A vector information processing apparatus comprising: a CPU comprising a plurality of asynchronously operating units (Knapp's Fig 1: #36, #38); a main memory for storing data (Knapp's Fig 1: #16); and a main memory controller for controlling the writing of data in said main memory (Knapp's #26 and #30), said main memory controller including a vector scatter (VSC) address buffer that holds a storage address in said main memory for each element designated by a vector scatter instruction (Knapp's Fig 3: #45, column 6 lines 5-18 describes fetching unit #44 fetching instruction and data from memory with multiple requests that are stored in the instruction bundle #45); wherein said main memory controller inhibits the outputting of a writing permission signal that permits writing to said main memory which is generated according to a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter

instruction if the writing request instructs storage of said element at an identical storage address as said at least one other element and the writing request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instructions (Knapp's column 6 line 66 to column 7 line 54 describe using of four CAMs structures to compare the source addresses fields of each instruction in the bundle to the in-flight instructions' destination address field; and detects the conflict "address matching" of instructions accessing memory in a sequence); wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from said asynchronously operating units of said CPU according to said vector scatter instruction (Knapp's column 5 lines 50-57 describes the instructions and sequence of actions of the different execution units Fig 1: #28 for instance ALU unit #36 and special purpose units to executing instructions for performing computations on array of data, column 5 lines 12-20; Knapp's column 6 lines 7-20 describes detecting the intra dependency of eight instructions I(0)-I(7) that corresponds to the claim's elements; and inter-dependency between the in-flight instructions). Knapp does not describe the multiple operation units operate in an asynchronously manner. However, Suzuki describes a processor with multiple arithmetic and logical units, Fig 11: #92 #93 blocks, these units can operate with different clocks as shown in Fig 1; These clocks are operated with different frequencies; Suzuki's column 3 lines 45-57; column 11 lines 48-51. It would have been obvious to one of ordinary skill in the art at the time of invention to include the clocking method as suggested by Suzuki in Knapp's system to allow logical units operating with clocks of different frequencies, thereby further optimizing and reducing the power consumption of the overall system (Suzuki's column 3 lines 50-58).

As for claim 2, the claim rejected based on the same rationale as in the rejection of claim 1. Knapp further describes wherein said main memory controller has a plurality of VSC address buffers corresponding respectively to said asynchronously operating units (Knapp's bundle #45, I (0)-I (7)).

As for claims 8-10, the claims recite wherein the number of storage addresses held by said VSC address buffer is set to at least (the number of elements simultaneously processed by said asynchronously operating unit)+1. Although Knapp and Suzuki do not describe the claim's detail of the size of the memory's received requests buffer. It is obviously that buffer size should be more that the number of requests being issued parallel from operating units of a processor in order to prevent the buffer being overflowed when receiving these requests simultaneously and in asynchronously manner.

Claim 11 rejected based on the same rationale as in the rejection of claim 1.

Claim 12 rejected based on the same rationale as in the rejection of claim 2.

Claims 19-20 recite writing requests for writing said element and said at least one other element to said storage address in said memory are issued respectively from different asynchronously operating units of said CPU according to said vector scatter instruction. The claims rejected based on the same rationale as in the rejection of claim 1.

Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al (US 6862676), Suzuki (US 6240524) as applied to claim 1, and further in view of Lee at el (US 6629271).

As for claim 4 the claims recites wherein said main memory controller comprises: a VSC address buffer controller for controlling said VSC address buffer to hold said storage address sent from said asynchronously operating units and, if an overflow condition occurs in said VCS address buffer, requests the asynchronously operating unit which has issued a vector scatter instruction that has caused said overflow to resend said element; and wherein said asynchronously operating unit has a retry buffer for holding each element designated by said vector scatter instruction issued thereby, and resends an element held by said retry buffer to said main memory controller if requested by said main memory controller to resend said element. Knapp and Suzuki do not describe the claim's detail of a retry buffer. However, Lee describes a processor with a replay system capable of keeping track of instructions being issued by the processor. Replay system detects the instructions that are not being executed properly and subsequently reissues them for re-execution (Lee's column 6, lines 27-45). It would have been obvious to one of ordinary skill in the art at the time of invention to include the retry technique as suggested by Lee in Knapp's system in order to re-executing the instructions in a proper order manner (Lee's column 6 lines 41-45; only retry those instructions not being completely executed).

Claims 15 rejected based on the same rationale as in the rejection of claim 4.

Allowable Subject Matter

Claims 3, 5-7,13-14,16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 3 recites "wherein said asynchronously operating units impart one identifier to a plurality of said writing requests issued according to a single vector scatter instruction, and said main memory controller clears the contents of said VSC address buffers if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other".

Claim 5 recites wherein said asynchronously operating units impart one identifier to a plurality of said writing requests issued according to a single vector scatter instruction, and said main memory controller clears the contents of said VSC address buffers if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

Claim 6 recites "wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting the timing to resend the element from said asynchronously operating unit to said asynchronously operating unit; and wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller".

The combination of above features is not found in the prior art of record.

Claims 7,17-18 have similar limitations as in claim 6.

Claims 13-14 have similar limitations as in claim 3.

Claim 16 have similar limitations as in claim 5.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Applicant's amendment filed 8/18/03 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
2/17/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER